4-Port USB HUB Controller **MSE9710**

Overview

The MSE9710 is a single chip 4-port Universal Serial Bus (USB) Hub controller that allows up to four USB devices and/or Hubs to connect to an upstream USB hub or USB host. The MSE9710 USB Hub Controller is highly integrated , requiring minimal external parts. The MSE9710 contains built-in transceivers, a 4X PLL clock generator with 12Mhz oscillator (requires an external 12Mhz crystal), power-on reset, per-port or ganged over current detection, per-port or ganged power switching and an on-board 3.3v regulator.

The MSE9710 is available in three different variations - MSE9710A, MSE9710B, MSE9710C - depending on how the descriptors are stored in the chip and each variation is available in both thru-hole and surface mount types. The thru-hole type comes in 30-pin SDIP package and the surface mount type comes in 32-pin TQFP package.

The MSE9710A variation has the contents of all descriptors hard-coded in the chip at the time of fabrication. Thus, none of the descriptor contents can be changed once the chips are made.

The MSE9710B variation contains eight different sets of descriptor contents hard-coded in the chip. This variation provides three pins which are used to select one of the eight descriptor sets stored in the chip.

The MSE9710C variation is same as MSE9710A plus the external serial EEPROM interface through which it reads 256 bytes of the descriptor contents stored in the external serial EEPROM. Using the EXTMEM pin, the user can select either the on-chip descriptors or descriptors stored in the external EEPROM. This variation gives the user the flexibility to change the descriptor contents without having to re-fabricate the chip.

Features

- Compliant with USB Protocol Revision 1.0
- No firmware required
- Four downstream ports
- Downstream device connect/disconnect detection
- Power management by supporting USB suspend/resume protocol
- Support for both low and full speed devices on the downstream ports
- Clock and data recovery from USB
- Bitstripping and Bitstuffing functions when the packets are addressed to the Hub
- CRC5 checking, CRC16 generation and checking for the packets addressed to the Hub
- Maintenance of the data toggle bits for the supported endpoints
- Output pin per-port for port power switching mode and input pin per-port for over-current detection
- External pin for selecting ganged or individual power switch mode
- External pin for selecting self-powered or bus-powered mode
- Built-in transceivers for upstream and downstream ports
- Built-in 3.3V voltage regulator
- Built-in 4X PLL clock generator

- Available in both 30-pin SDIP and 32-pin TQFP packages

MSE9710A 30-pin SDIP Pinouts

Pin No.	Pin Name	I/O Type	Description
1	AVDD	POWER	Analog Power for Voltage Regulator.
2	XOUT	OUT	Oscillator Output.
3	XIN	IN	Oscillator Input.
4	AGND	POWER	Analog Ground for PLL ONLY. Analog Ground for Other Blocks.
5	PVDD	POWER	Analog Power for PLL ONLY.
6	TESTn	IN	For Test.
7	DP4_PWRONn	OUT	When TESTn is low, this pin will be output of the Analog PLL(48MHz). When TESTn is high, Power Control Signal for DP4.
8	DP4_OCn	IN	Over Current Indication Signal for DP4.
9	DP4_DM	IN/OUT	D- for DP4.
10	DP4_DP	IN/OUT	D+ for DP4.
11	DP3_PWRONn	OUT	Power Control Signal for DP3.
12	DP3_OCn	IN	Over Current Indication Signal for DP3.
13	DP3_DM	IN/OUT	D- for DP3.
14	DP3_DP	IN/OUT	D+ for DP3.
15	DP2_PWRONn	OUT	Power Control Signal for DP2
16	DP2_OCn	IN	Over Current Indication Signal for DP2
17	DP2_DM	IN/OUT	D- for DP2.
18	DP2_DP	IN/OUT	D+ for DP2.
19	VDD	POWER	Power for Digital Core. Power for I/O PAD.
20	GND	POWER	Ground for Digital Core. Ground for I/O PAD.
21	DP1_PWRONn	OUT	Power Control Signal for DP1.
22	DP1_OCn	IN	Over Current Indication Signal for DP1.
23	DP1_DM	IN/OUT	D- for DP1.
24	DP1_DP	IN/OUT	D+ for DP1.

25	RP_DM	IN/OUT	D- for Root Port.
26	RP_DP	IN/OUT	D+ for Root Port.
27	RESETn	IN	Reset Signal.
28	SELF_PWR	IN	"1" => Self-powered. "0" => Bus-powered.
29	PWR_SW	IN	"1" => Ganged Power Switching & Global Over-current Protection. "0" => Individual Port Power Switching & Individual Port Over-current Protection.
30	V3P3	OUT	3.3V Voltage Regulator Output.

MSE9710A 32-pin TQFP Pinouts

Pin No.	Pin Name	I/O Type	Description
1	PVDD	POWER	Analog Power for PLL ONLY.
2	TESTn	IN	For Test.
3	DP4_PWRONn	OUT	When TESTn is low, this pin will be output of the Analog PLL(48MHz). When TESTn is high, Power Control Signal for DP4.
4	DP4_OCn	IN	Over Current Indication Signal for DP4.
5	DP4_DM	IN/OUT	D- for DP4.
6	DP4_DP	IN/OUT	D+ for DP4.
7	DP3_PWRONn	OUT	Power Control Signal for DP3.
8	DP3_OCn	IN	Over Current Indication Signal for DP3.
9	DP3_DM	IN/OUT	D- for DP3.
10	DP3_DP	IN/OUT	D+ for DP3.
11	DP2_PWRONn	OUT	Power Control Signal for DP2
12	DP2_OCn	IN	Over Current Indication Signal for DP2
13	DP2_DM	IN/OUT	D- for DP2.
14	DP2_DP	IN/OUT	D+ for DP2.
15	VDD	POWER	Power for Digital Core. Power for I/O PAD.
16	GND1	POWER	Ground for Digital Core. Ground for I/O PAD.

17	SUSPEND	OUT	Suspend Indication Signal.
18	DP1_PWRONn	OUT	Power Control Signal for DP1.
19	DP1_OCn	IN	Over Current Indication Signal for DP1.
20	DP1_DM	IN/OUT	D- for DP1.
21	DP1_DP	IN/OUT	D+ for DP1.
22	RP_DM	IN/OUT	D- for Root Port.
23	RP_DP	IN/OUT	D+ for Root Port.
24	RESETn	IN	Reset Signal.
25	SELF_PWR	IN	"1" => Self-powered. "0" => Bus-powered.
26	PWR_SW	IN	"1" => Ganged Power Switching & Global Over-current Protection. "0" => Individual Port Power Switching & Individual Port Over-current Protection.
27	V3P3	OUT	3.3V Voltage Regulator Output.
28	AVDD	POWER	Analog Power for Voltage Regulator.
29	XOUT	OUT	Oscillator Output.
30	XIN	IN	Oscillator Input.
31	AGND1	POWER	Analog Ground.
32	AGND2	POWER	Analog Ground for PLL Only

MSE9710B 30-pin SDIP Pinouts

Pin No.	Pin Name	I/O Type	Description
1	AVDD	POWER	Analog Power for Voltage Regulator.
2	XOUT	OUT	Oscillator Output.
3	XIN	IN	Oscillator Input.
4	AGND	POWER	Analog Ground for PLL ONLY. Analog Ground for Other Blocks.
5	PVDD	POWER	Analog Power for PLL ONLY.
6	TESTn	IN	For Test.
7	DP4_PWRONn	OUT	When TESTn is low, this pin will be output of the Analog PLL(48MHz). When TESTn is high, Power Control Signal for DP4.
8	DP4_OCn	IN	Over Current Indication Signal for DP4. When TESTn is low, this pin will be used for

			"RESET" input.
9	DP4_DM	IN/OUT	D- for DP4.
10	DP4_DP	IN/OUT	D+ for DP4.
11	DP3_PWRONn	OUT	Power Control Signal for DP3.
12	DP3_OCn	IN	Over Current Indication Signal for DP3.
13	DP3_DM	IN/OUT	D- for DP3.
14	DP3_DP	IN/OUT	D+ for DP3.
15	DP2_PWRONn	OUT	Power Control Signal for DP2
16	DP2_OCn	IN	Over Current Indication Signal for DP2
17	DP2_DM	IN/OUT	D- for DP2.
18	DP2_DP	IN/OUT	D+ for DP2.
19	VDD	POWER	Power for Digital Core. Power for I/O PAD.
20	GND	POWER	Ground for Digital Core. Ground for I/O PAD.
21	DP1_PWRONn	OUT	Power Control Signal for DP1.
22	DP1_OCn	IN	Over Current Indication Signal for DP1.
23	DP1_DM	IN/OUT	D- for DP1.
24	DP1_DP	IN/OUT	D+ for DP1.
25	RP_DM	IN/OUT	D- for Root Port.
26	RP_DP	IN/OUT	D+ for Root Port.
27	IDSEL_1	IN	User Configuration Select Signal. IDSEL_3 IDSEL_2 IDSEL_1 0 0 0 => User 1 0 0 1 => User 2 0 1 0 => User 3 0 1 1 => User 4 1 0 0 => User 5 1 0 1 => User 6 1 1 0 => User 7 1 1 1 => User 8
28	IDSEL_2	IN	User Configuration Select Signal.
29	IDSEL_3	IN	User Configuration Select Signal.
30	V3P3	OUT	3.3V Voltage Regulator Output.

MSE9710B 32-pin TQFP Pinouts

Pin	Pin Name	I/O Type	Description

No.			
1	PVDD	POWER	Analog Power for PLL ONLY.
2	TESTn	IN	For Test.
3	DP4_PWRONn	OUT	When TESTn is low, this pin will be output of the Analog PLL(48MHz). When TESTn is high, Power Control Signal for DP4.
4	DP4_OCn	IN	Over Current Indication Signal for DP4.
5	DP4_DM	IN/OUT	D- for DP4.
6	DP4_DP	IN/OUT	D+ for DP4.
7	DP3_PWRONn	OUT	Power Control Signal for DP3.
8	DP3_OCn	IN	Over Current Indication Signal for DP3.
9	DP3_DM	IN/OUT	D- for DP3.
10	DP3_DP	IN/OUT	D+ for DP3.
11	DP2_PWRONn	OUT	Power Control Signal for DP2
12	DP2_OCn	IN	Over Current Indication Signal for DP2
13	DP2_DM	IN/OUT	D- for DP2.
14	DP2_DP	IN/OUT	D+ for DP2.
15	VDD	POWER	Power for Digital Core. Power for I/O PAD.
16	GND1	POWER	Ground for Digital Core. Ground for I/O PAD.
17	SUSPEND	OUT	Suspend Indication Signal.
18	DP1_PWRONn	OUT	Power Control Signal for DP1.
19	DP1_OCn	IN	Over Current Indication Signal for DP1.
20	DP1_DM	IN/OUT	D- for DP1.
21	DP1_DP	IN/OUT	D+ for DP1.
22	RP_DM	IN/OUT	D- for Root Port.
23	RP_DP	IN/OUT	D+ for Root Port.
24	IDSEL_1	IN	User Configuration Select Signal. IDSEL_3 IDSEL_2 IDSEL_1 0 0 0 => User 1 0 0 1 => User 2 0 1 0 => User 3 0 1 1 => User 4 1 0 0 => User 5 1 0 1 => User 6 1 1 0 => User 7 1 1 1 => User 8
25	IDSEL_2	IN	User Configuration Select Signal.
26	IDSEL_3	IN	User Configuration Select Signal.
27	V3P3	OUT	3.3V Voltage Regulator Output.

28	AVDD	POWER	Analog Power for Voltage Regulator.
29	XOUT	OUT	Oscillator Output.
30	XIN	IN	Oscillator Input.
31	AGND1	POWER	Analog Ground.
32	AGND2	POWER	Analog Ground for PLL only

MSE9710C 30-pin SDIP Pinouts

Pin No.	Pin Name	I/O Type	Description
1	AVDD	POWER	Analog Power for Voltage Regulator.
2	XOUT	OUT	Oscillator Output.
3	XIN	IN	Oscillator Input.
4	AGND	POWER	Analog Ground for PLL ONLY. Analog Ground for Other Blocks.
5	PVDD	POWER	Analog Power for PLL ONLY.
6	TESTn	IN	For Test.
7	DP4_PWRONn	OUT	When TESTn is low, this pin will be output of the Analog PLL(48MHz). When TESTn is high, Power Control Signal for DP4.
8	DP4_OCn	IN	Over Current Indication Signal for DP4. When TESTn is low, this pin will be used for "RESET" input.
9	DP4_DM	IN/OUT	D- for DP4.
10	DP4_DP	IN/OUT	D+ for DP4.
11	DP3_PWRONn	OUT	Power Control Signal for DP3.
12	DP3_OCn	IN	Over Current Indication Signal for DP3.
13	DP3_DM	IN/OUT	D- for DP3.
14	DP3_DP	IN/OUT	D+ for DP3.
15	DP2_PWRONn	OUT	Power Control Signal for DP2
16	DP2_OCn	IN	Over Current Indication Signal for DP2
17	DP2_DM	IN/OUT	D- for DP2.
18	DP2_DP	IN/OUT	D+ for DP2.
19	VDD	POWER	Power for Digital Core. Power for I/O PAD.
20	GND	POWER	Ground for Digital Core. Ground for I/O PAD.

21	DP1_PWRONn	OUT	Power Control Signal for DP1.
22	DP1_OCn	IN	Over Current Indication Signal for DP1.
23	DP1_DM	IN/OUT	D- for DP1.
24	DP1_DP	IN/OUT	D+ for DP1.
25	RP_DM	IN/OUT	D- for Root Port.
26	RP_DP	IN/OUT	D+ for Root Port.
27	EXTMEM	IN	External EPROM Read Enable Signal.
28	EPCLK/ SELF_PWR	IN/OUT	When "EXTMEM" is high : Serial Clock Output to the external EPROM. When "EXTMEM" is low : "1" => Self-powered, "0" => Bus-powered.

MSE9710C 32-pin TQFP Pinouts

Pin No.	Pin Name	I/O Type	Description
1	PVDD	POWER	Analog Power for PLL ONLY.
2	TESTn	IN	For Test.
3	DP4_PWRONn	OUT	When TESTn is low, this pin will be output of the Analog PLL(48MHz). When TESTn is high, Power Control Signal for DP4.
4	DP4_OCn	IN	Over Current Indication Signal for DP4.
5	DP4_DM	IN/OUT	D- for DP4.
6	DP4_DP	IN/OUT	D+ for DP4.
7	DP3_PWRONn	OUT	Power Control Signal for DP3.
8	DP3_OCn	IN	Over Current Indication Signal for DP3.
9	DP3_DM	IN/OUT	D- for DP3.
10	DP3_DP	IN/OUT	D+ for DP3.
11	DP2_PWRONn	OUT	Power Control Signal for DP2
12	DP2_OCn	IN	Over Current Indication Signal for DP2
13	DP2_DM	IN/OUT	D- for DP2.
14	DP2_DP	IN/OUT	D+ for DP2.
15	VDD	POWER	Power for Digital Core. Power for I/O PAD.
16	GND1	POWER	Ground for Digital Core. Ground for I/O PAD.
17	SUSPEND	OUT	Suspend Indication Signal.

18	DP1_PWRONn	OUT	Power Control Signal for DP1.
19	DP1_OCn	IN	Over Current Indication Signal for DP1.
20	DP1_DM	IN/OUT	D- for DP1.
21	DP1_DP	IN/OUT	D+ for DP1.
22	RP_DM	IN/OUT	D- for Root Port.
23	RP_DP	IN/OUT	D+ for Root Port.
24	EXTMEM	IN	External EPROM Read Enable Signal.
25	EPCLK/ SELF_PWR	IN/OUT	When “EXTMEM” is high : Serial Clock Output to the external EPROM. When “EXTMEM” is low : “1” => Slef-powered, “0” => Bus-powered.
26	EPDATA/ PWR_SW	IN/OUT	When “EXTMEM” is high : Serial Data to/from the external EPROM. When “EXTMEM” is low : “1” => Ganged Power Switching & Global Over-current Protection. “0” => Individual Port Power Switching & Individual Port Over-current Protecton.
27	V3P3	OUT	3.3V Voltage Regulator Output.
28	AVDD	POWER	Analog Power for Voltage Regulator.
29	XOUT	OUT	Oscillator Output.
30	XIN	IN	Oscillator Input.
31	AGND1	POWER	Analog Ground.
32	AGND2	POWER	Analog Ground for PLL only